SuperGen ORE Hub ECR Fund Report

Wide-Bandgap-Enabled Dynamic Braking System for Grid Integration of Offshore Wind Farms

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Key notes: This report indicates the findings of the SuperGen ORE Hub ECR Fund enabled by the ORE hub. By means of modelings and analysis, it was shown that pole-to-pole DC faults on HB-MMC-VSC-HVDC schemes impose significant risk of cascade failure on IGBT/diode pairs. Other novel topologies with fault blocking capability, i.e. AAC converters, and DC circuit breakers are not yet fully matured. Therefore, silicon thyristors are used to bypass the DC faults until AC breakers activate. However, silicon thyristors are also at risk of failure due to the capacitor voltage collapse at high junction temperatures caused due to imbalanced reverse recovery current conduction. Hence, the recovery cycles are included as part of IEC standard 62501 HVDC type-test program. Emergence of commercial Silicon Carbide (SiC) thyristors has the potential to tackle this risk. The results of these findings were reported in a paper published by the IEEE Open Journal on Power Electronics, and the support provided by the partner & SuperGen ORE Hub ECR Fund was acknowledged. The paper can be found in reference 1.

Synopsis:

We have investigated the opportunities and challenges of implementation of SiC thyristors by accurately modeling the performance of thyristors at fault. It was seen that SiC thyristors with acceptable surge current and reverse blocking capability can eliminate the failure mode of silicon thyristors due to minimal recovery stored charge, resulting in an equal share of reverse voltage on all thyristors. SiC thyristors can alleviate the electro-thermal stress on the silicon thyristors following bypass of a DC fault current. The ability of SiC thyristors to tackle this stress is predicated upon the low stored recovery charge in the drift region of the device which enables a fast reverse recovery transient. Consequently, the reverse voltage on all thyristors is kept at its minimum, especially when the thyristors suffer from a high junction temperature due to bypassing a significant proportion of surge current as in Fig.1.

To date majority of SiC thyristors are designed with asymmetrical blocking capability in favour of forward voltage blocking to minimize the on-state voltage drop. In contrast, the reverse blocking capability is the key parameter when used in protection of HB-MMC-VSC-HVDC. Therefore, device structures which are designed in favour of reverse blocking capability are sought. The surge current of the SiC thyristors also need to increase, which would depend on production of defect-free substrates. These are expected to be available in foreseeable future. Therefore, it can be argued that production of high current SiC thyristors with considerable reverse blocking capability will eliminate the main failure risk associated with the use of silicon thyristors and can displace the silicon thyristors and other complex fault management techniques in protection of HB-MMC-VSC-HVDC converters at DC faults.

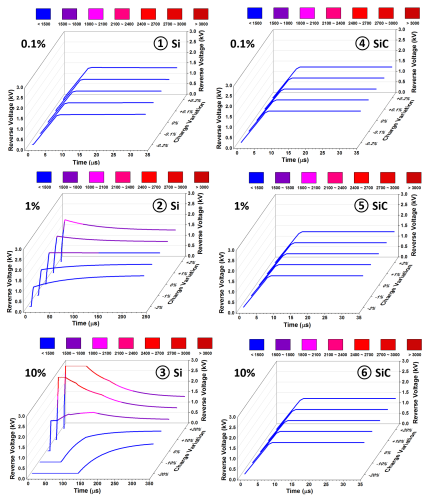

Figure 1: The reverse voltage depending on recovery charge variations for 1–3. silicon thyristors and 4-6. SiC thyristors.

References

[1] C. Shen, S. Jahdi, O. Alatise, J. Ortiz-Gonzalez, A. Aithal and P. Mellor, “Prospects and Challenges of 4H-SiC Thyristors in Protection of HB-MMC-VSC-HVDC Converters,” in IEEE Open Journal of Power Electronics, vol. 2, pp. 145-154, 2021.
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