Report to the SuperGen ORE Hub ECR Fund

Optimisation of Compact Wide-Bandgap-Enabled Power Electronic Converters for Offshore Wind Farms

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Offshore wind farms are an essential part of tackling the global climate emergency. However, given their inhospitable and inaccessible locations, they require higher standards of performance and reliability to keep the operational costs sustainable. Typical offshore windfarms generate 900 MW AC, which is converted to +/-320 kV DC via modular multi-level converters (MMC). These converters are traditionally implemented with multiple half-bridge modules, composed of a high number of silicon devices. These devices restrict the converter switching frequency to 200 Hz, as increasing further would cause significant power losses and require a substantial cooling system. All this increases the area footprint and thus the total cost of the offshore power converter substation.

Fortunately, the introduction of wide-bandgap devices, like silicon carbide (SiC), to the power semi-conductor market helps overcome the limitations of traditional silicon. While more expensive, SiC has superior qualities that reduce the overall converter volume and results in off-shore substations that are more compact and thus less expensive to manufacture and maintain. This project investigated the use of SiC devices in offshore wind farm substations and developed tools that holistically optimise the system to ensure the most compact power electronic converter for this application.

An optimisation study was done on the converter topology used primarily in offshore wind platforms, the half-bridge submodule modular multi-level converter (HBSM-MMC). The HBSM-MMC is suited to the high voltage direct current (HVDC) transmission used in offshore wind systems, due to its high voltage capability, low AC side harmonics and high fault tolerance. However, this requires a high part count, as the HBSM-MMC is typically implemented with silicon IGBT/thyristor pairs connected in series to achieve the desired voltage level. The increased device count reduces the harmonics and the line filter volume, but it increases the device losses, the size of the cooling system and results in a larger overall converter volume. The losses and cooling system can be reduced by lowering the switching frequency, however this increases the severity of EMI issues and thus requires larger line filters.

SiC MOSFETs, overcome these trade-off compromises but only if the converter can be designed holistically. To realise this an optimisation tool was developed that models the converter's power losses for a range of key operational parameters. For the HBSM-MMC, these parameters include the switching devices, number of levels and switching frequency. The tool modelled the conduction and switching losses by assuming the converter operates with phase disposition pulse width modulation (PD-PWM). Potential devices are parameterized using datasheet information and the user inputs key specifications, such as power rating and DC-link voltage. A generalised N-level model using PD-PWM, was developed for the tool so that power losses for a range of levels could be quickly and accurately calculated without resorting to intensive simulation.

The total conduction and switching losses calculated by the tool for a specified HBSM-MMC is shown in Fig. 1 for various combinations of switching frequency, level number and SiC MOSFET. The results were verified through detailed PLECS simulation where the conduction and switching loss error rate was 1.3% and 2.5%. Some discrepancy results from the tool assuming the devices conduct during specific intervals, whereas the MMC's capacitor balancing algorithm results in random conduction. Nevertheless, the accuracy is sufficient as a foundation for holistic design optimisation of the MMC.

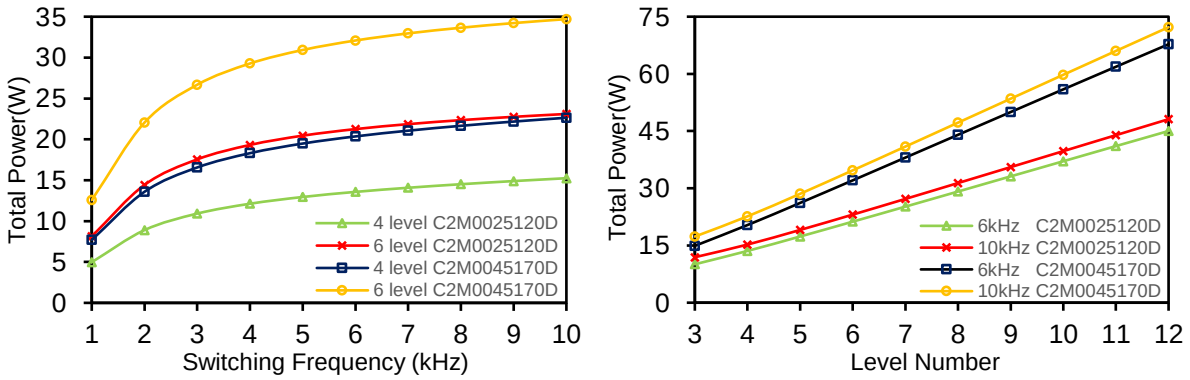

Fig. 1. Total power loss of sample SiC devices for varying switching frequency and level number

Another study was done on the optimisation of the design of SiC MOSFETs. SiC devices have a higher critical electric field than that of silicon, allowing them to block higher voltages for a thinner drift region. Silicon power MOSFETs suffer from high on-state resistance resulting in high conduction losses. Thus, a new generation of devices called Silicon superjunction MOSFETs were introduced that can block high voltages with a thinner and less resistive drift region.

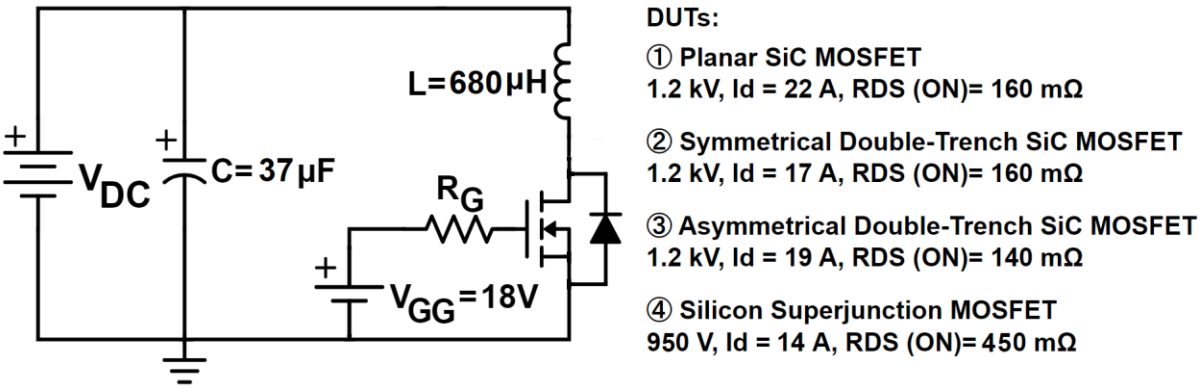

Fig. 2. Schematic of Unclamped inductive switching (UIS) test and DUTs.

As the reliability of devices in an irregular condition is of a crucial importance, avalanche failure mechanisms and capability of devices are evaluated by utilizing the unclamped inductive switching (UIS) test based of Fig. 2 in which a single gate pulse with duration of 40 µs is applied to the device. The avalanche energy density of the devices calculated from the UIS test is shown in Fig. 3. Asymmetrical double-trench SiC MOSFET has the largest avalanche energy density, followed by Symmetrical double-trench SiC MOSFET. At room temperature Symmetrical double-trench SiC MOSFET is more rugged than the others as it fails at a higher DC link voltage and sustains higher critical avalanche energy before failure. At high temperatures (175°C) Asymmetrical double-trench SiC MOSFET is more rugged for the same reason. For the high temperature tests, the threshold voltage, which is a temperature sensitive parameter, has been reduced due to the intrinsic charge carrier density having a positive temperature coefficient together with interface charge traps.

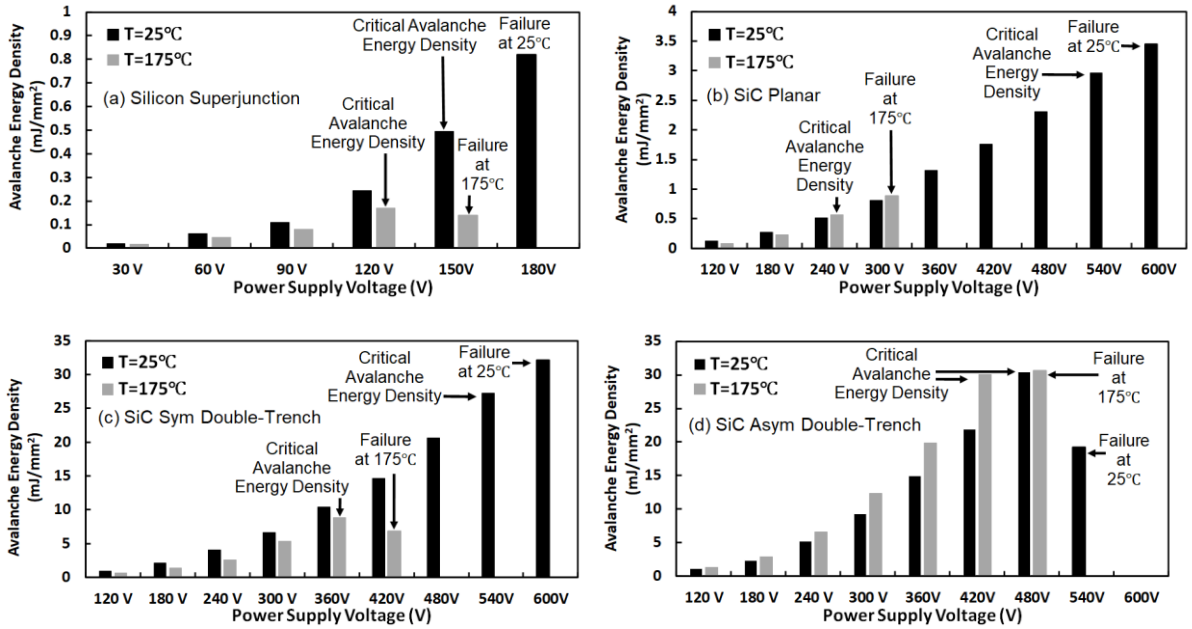

Fig. 3. UIS test avalanche energy density of the four devices for various DC-link voltage at 25°C and 175°C.