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Optimisation of Compact Wide-Bandgap-Enabled Power Electronic Converters for Offshore Wind Farms

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Offshore wind farms are an essential part of tackling the global climate emergency. However, given their inhospitable and inaccessible location, they need higher performance and reliability to keep the operational costs sustainable. Typical offshore windfarms generate 900 MW AC, which is converted to +/-320 kV DC via modular multi-level converters (MMC). These converters are traditionally implemented with multiple silicon devices that result in significant power losses and a high area footprint of the offshore power converter substation.

Fortunately, the introduction of wide-bandgap devices, like silicon carbide (SiC), to the power semiconductor market helps overcome the limitations of traditional silicon. While more expensive, SiC has superior qualities that reduce the overall converter volume and thus make offshore substations more compact and less expensive to manufacture and maintain.

An optimisation study was done on the converter topology used primarily in offshore wind platforms, the half-bridge submodule modular multi-level converter (HBSM-MMC). The HBSM-MMC is suited to the high voltage direct current (HVDC) transmission used in offshore wind systems, due to its high voltage capability, EMI performance and fault tolerance, however this comes at the cost of a high semiconductor part count, increased losses and increased converter volume.

SiC MOSFETs overcome these trade-off compromises but only if the converter is designed holistically. To realise this an optimisation tool was developed that quickly and accurately predicted the converter's power losses for a range of key operational parameters. Power losses predicted by the tool for some specified HBSM-MMCs is shown in Fig. 1. The results are used as a foundation for holistic design optimisation.

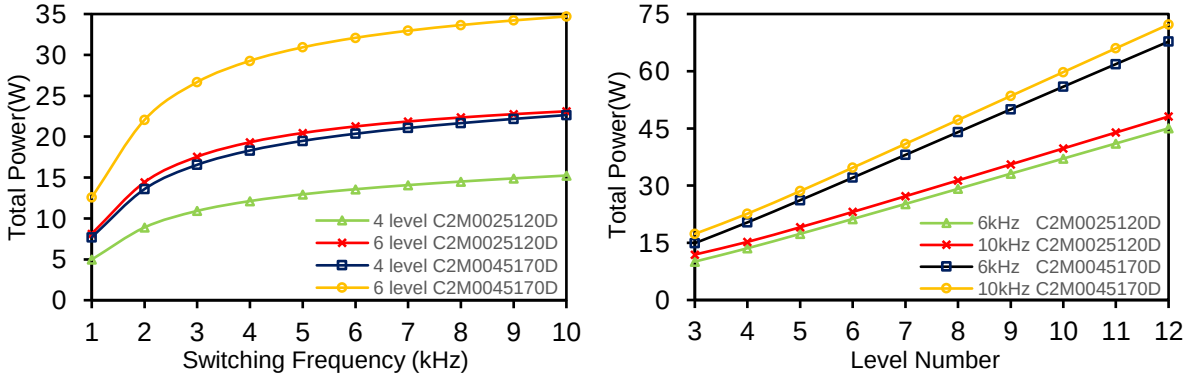

Fig. 1. Total power loss of sample SiC devices for varying switching frequency and level number

Another study was done on the optimisation of the design of SiC MOSFETs. As the reliability of devices in an irregular condition is of a crucial importance, avalanche failure mechanisms and capability of devices are evaluated by utilizing the unclamped inductive switching (UIS) test. Fig. 2 depicts the test setup of this experiment in which a single gate pulse with duration of 40 µs is applied to the device.

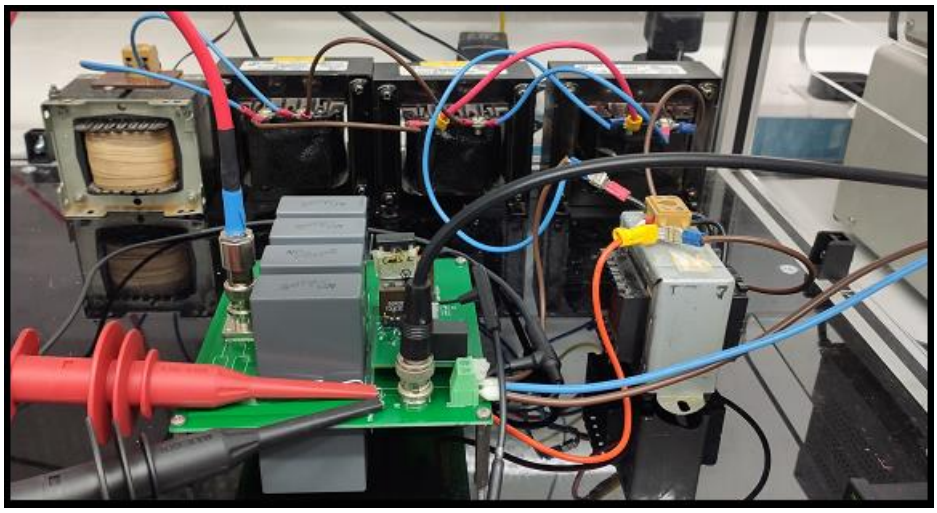

Fig. 2. Experimental test setup of the Unclamped inductive switching test board.

Fig. 3 show the waveforms of avalanche drain-source voltage and avalanche load current of the devices at 25°C while Fig. 4 shows this for 175°C. It can be seen that the rate of failure of Silicon superjunction, SiC planar and Asymmetrical double-trench MOSFETs is higher than the symmetrical double-trench MOSFET at 25°C. Moreover, Silicon Superjunction MOSFET and the Asymmetrical double-trench MOSFET fail at lower DC-link voltage compared to the two other ones. By increasing the temperature all the four devices fail at lower DC-link voltages, but Silicon superjunction and SiC planar MOSFET are influenced more. By increasing the temperature from 25°C to 175°C avalanche failure happens in lower DC-link voltage in all cases which is justifiable. For example, in BJT latch-up mechanism, because of the positive and negative coefficient of the resistance and voltage drop of BJT, the BJT will be triggered sooner as the temperature increases. The symmetrical double-trench MOSFET can withstand higher critical avalanche energy (the maximum avalanche energy that a device can sustain before failure) compared to others.

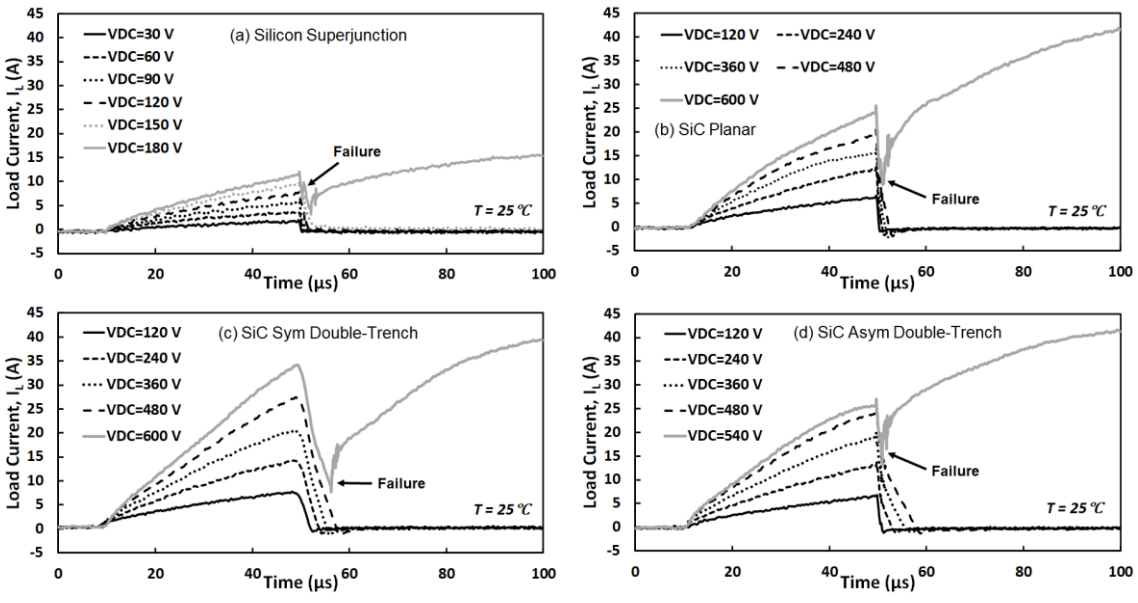

Fig. 3. Avalanche load current of the four devices for various DC-link voltage until the devices failed at 25°C.

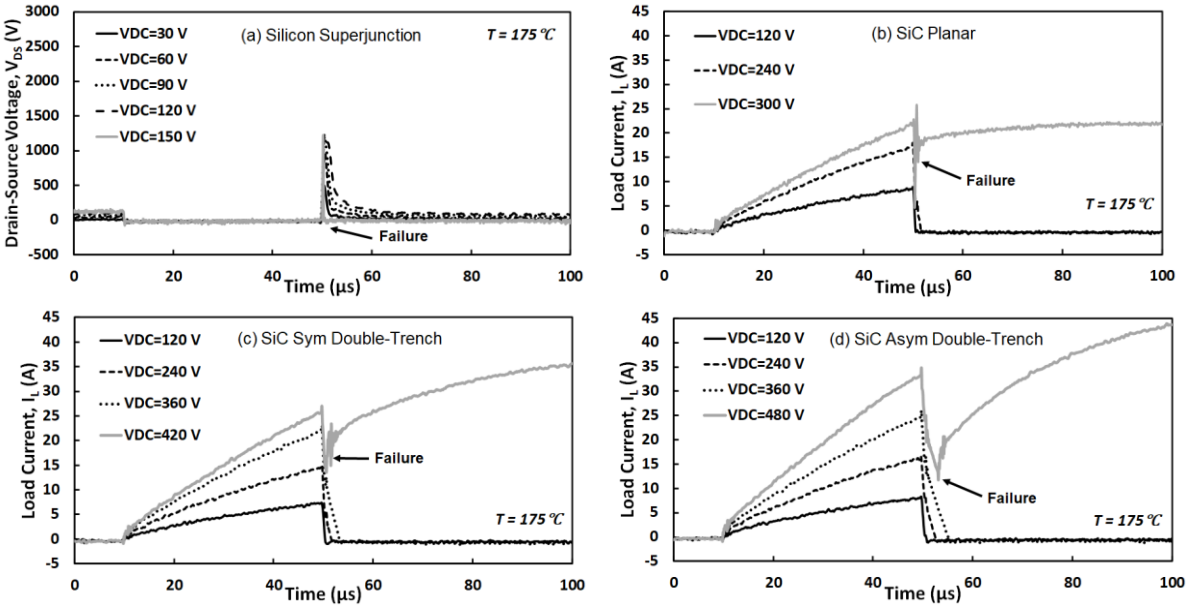

Fig. 4. Avalanche load current of the four devices for various DC-link voltage until the devices failed at 175°C.