University of BRISTOL

Optimisation of Compact Wide-Bandgap-Enabled Power Electronics Converters for Offshore Wind Farms

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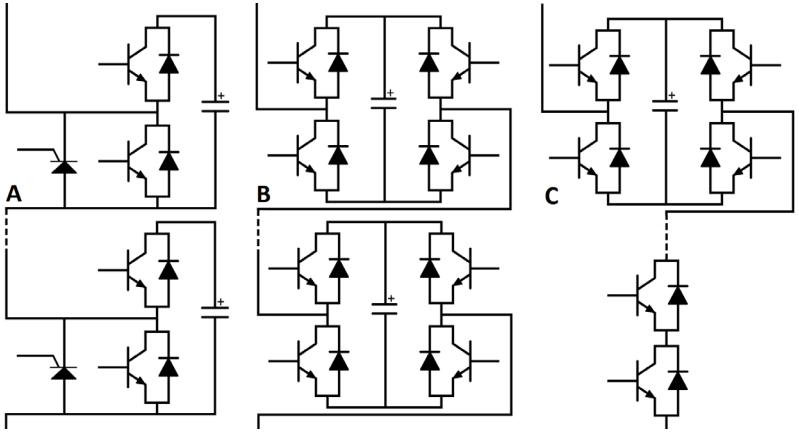
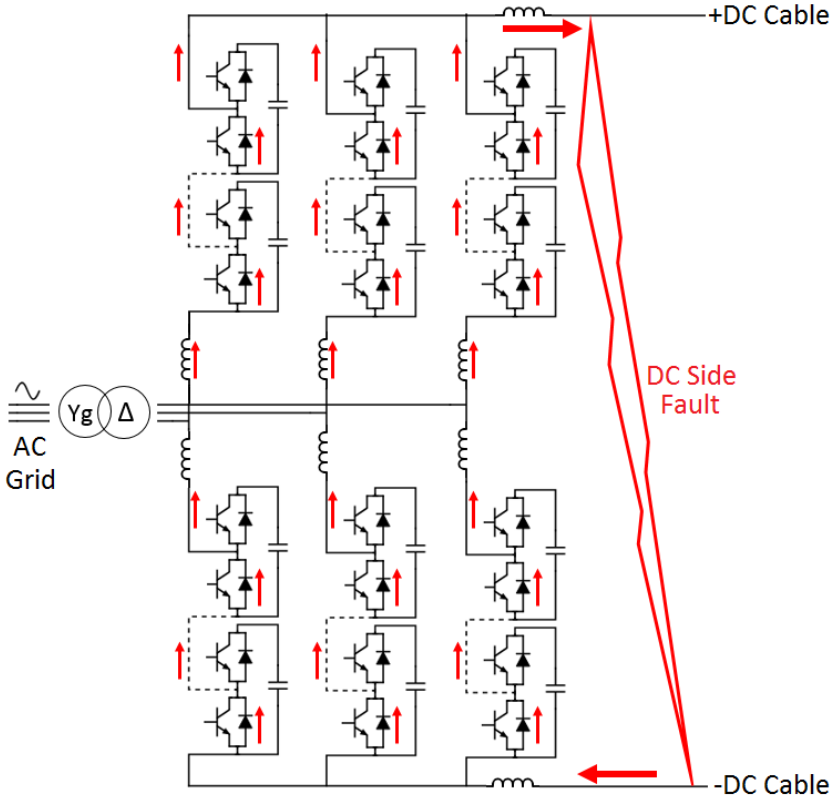
Introduction:

- Initial VSC-HVDC converters had 2-level and 3-level structures.
- These were simpler to control.
- Many challenges as hundreds of series-connected devices had to be switched simultaneously.
- MMC converters remove this issue.



MMC-VSC-HVDC CONVERTERS AT DC FAULTS:

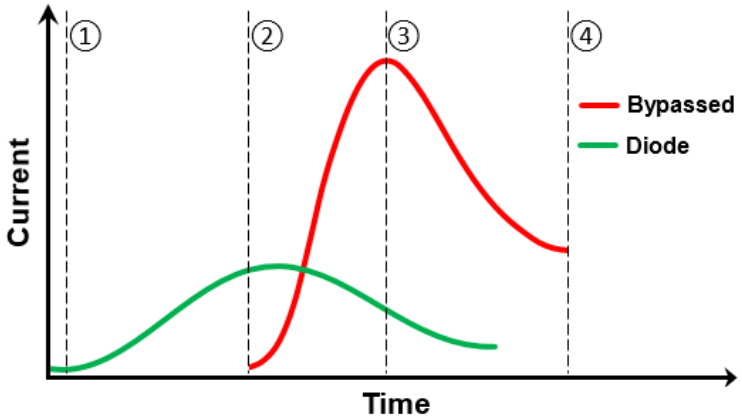
- Pole-to-pole DC fault imposes a significant risk.
- DC cable fault is rare, however more likely when overhead lines are used.
- The bottom anti-parallel diode provides a low resistance path for the DC fault current to circulate across all bottom IGBT/diode modules.



MMC-VSC-HVDC CONVERTERS AT DC FAULTS:

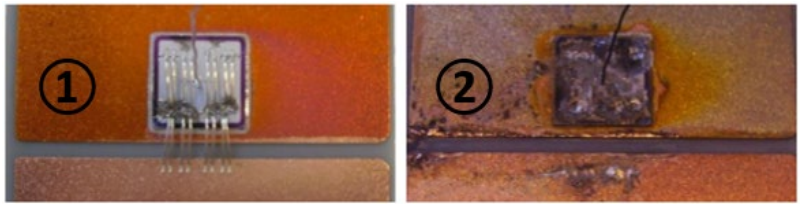
- The bypass thyristor will not mitigate the fault current but will provide a safe bypass path.
- As soon as the current in each arm reaches a pre-defined value, the thyristors will be fired, and the current is diverted.

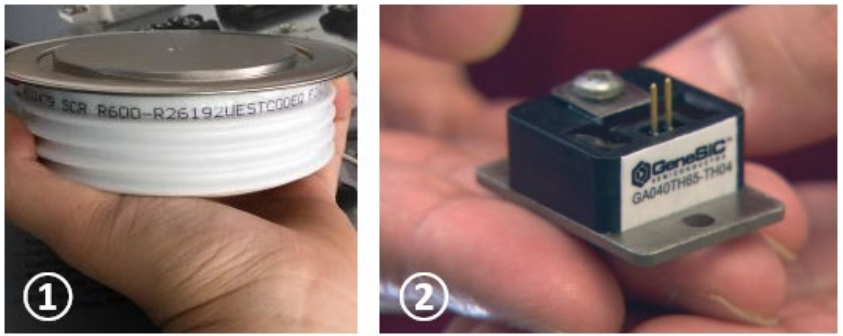
- The steps to mitigate the current are:
  1. DC fault starts to rise in the diode.
  2. Current reaches pre-defined value
  3. Fault increases while bypassed in thyristors.
  4. AC breakers disconnect.



STATE OF THE ART OF SIC THYRISTORS

- Failure in devices can be either in open-circuit mode or short-circuit mode. The latter is more risky.
- The typical 4-inch 6.5 kV Silicon thyristor disk and 6.5 kV Silicon Carbide thyristor in SOT-227 package with 8.2*8.2 mm die area cut from a 3 inch 4H-SiC wafer can be seen.

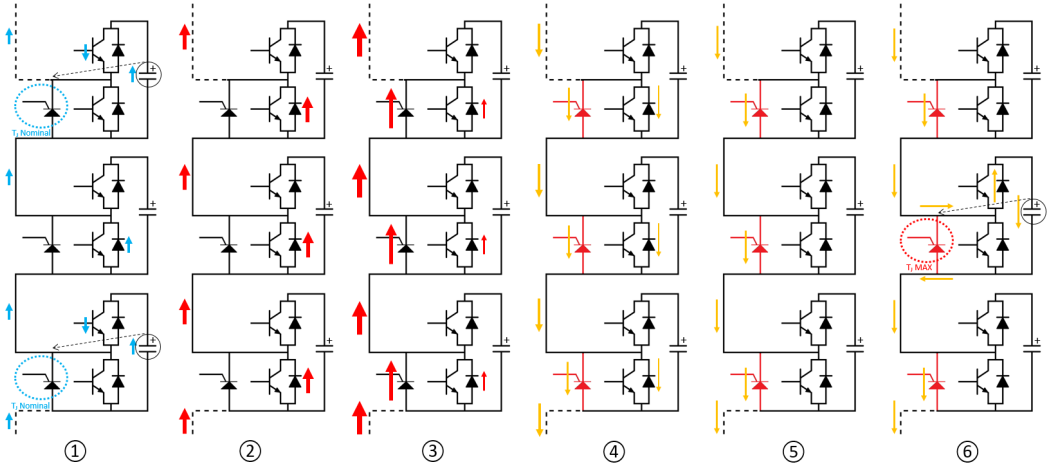




SIC THYRISTORS AS HB-MMC PROTECTION

The sequence of events in protection against a DC fault is as follows:

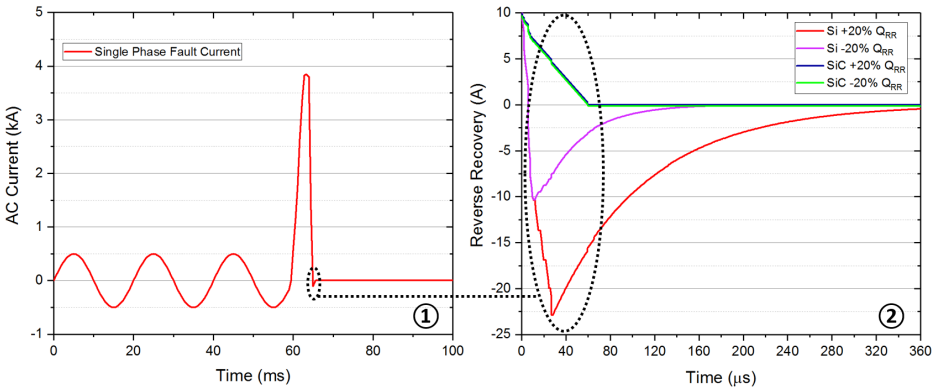
1. Normal operation
2. Instigation of Fault
3. Thyristors Fired
4. Fault removed, and devices recover
5. All diodes recovered, and Thyristors continue to recover
6. 6. Some thyristors recovered while others are still recovering.



MODELING THYRISTORS AT DC FAULTS:

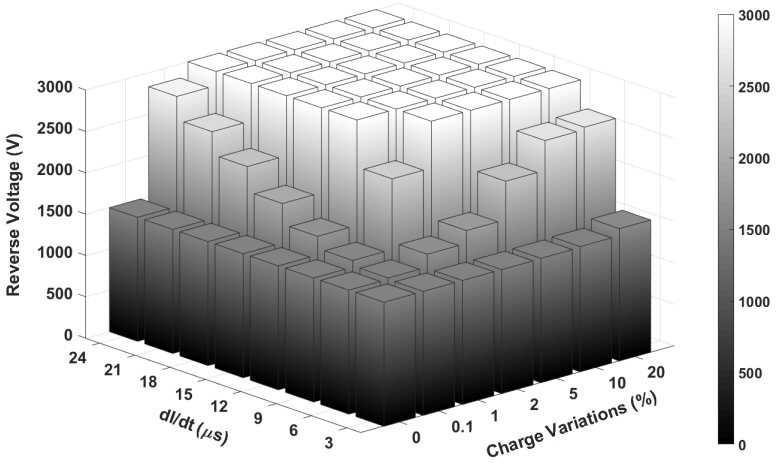
It can be seen that:

1. Synthesized fault current
2. Reverse recovery current in silicon and SiC thyristor at +20% and -20% charge profiles.



MODELING THYRISTORS AT DC FAULTS:

- 3D plot of the worst-case reverse voltage depending on recovery charge variations and fault dIF/dt of silicon device. N.B., the SiC thyristor reverse voltage is constant at 1.5 kV.
- The increase of dIF/dt or charge difference rapidly results in additional reverse blocking requirement on the fast-recovered silicon thyristors, while the reverse voltage for SiC device consistently remains at its share of DC line-to-line voltage, irrespective of capacitor voltage, charge variation or dIF/dt.



Conclusions

- SiC thyristors can relax the electro-thermal stress on the silicon thyristors following bypassing of a DC fault current.
- The key feature in SiC thyristors enabling them to tackle this stress is the very low stored recovery charge in the drift region of device.
- SiC thyristors are designed with asymmetrical blocking capability.
- Symmetrical or asymmetrical structures which are designed in favour of reverse blocking capability are sought. The surge current of the devices also need to increase, which depend on production of defect-free substrates. These are expected to be available in foreseeable future.
- It can be argued that production of high current SiC thyristors with considerable reverse blocking capability will eliminate the main failure risk of silicon thyristors and will displace the silicon thyristors and other complex fault management techniques in protection of HB-MMC-VSC-HVDC converters at DC faults.

Future Work

- Ongoing development of an optimisation tool that demonstrates the efficiency improvement and volume reduction that can be achieved in a MMC-VSC-HVDC converter when SiC devices are used in place of silicon devices
- Investigating the effect the trade-off between number of levels, number of series connected devices and device ratings has on converter efficiency, passive component sizing, electromagnetic compatibility (EMC) and thermal performance
- Design and fabricate a converter prototype to verify the accuracy of the optimisation tool

References

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